Synchronization Design of a Coupled Phase-Locked Loop

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***Abstract*—Coupled phase-locked loops (CPLLs) are introduced as novel circuits for phased-array antennas. Successful implementation relies on characterizing the synchronization behavior of CPLL circuits over a broad range of circuit parameters. Considering inherent time delay in the phase-locked loop demonstrates the degradation in the pull-in and hold-in ranges, as well as circuit instabilities, suggesting circuit parameter limits in a phased-array design. We compare the theoretical limits, in the form of analytic equations and numerical simulations, with measurements of the pull-in and hold-in processes of a 1.5-GHz prototype CPLL.**

***Index Terms*—Coupled phase-locked loop (CPLL), hold-in range, pull-in range, time delay.**

I. Introduction

An investigation into alternate phased-array antenna topologies has spurred interest in coupled phase-locked loops (CPLLs). Phased-array antennas rely on tunable phase relationships between neighboring antenna elements to develop narrow beamwidth radiation patterns. York and Itoh [1], Pogorzelski *et al.* [2], and Chang *et al.* [9] demonstrated the potential for coupled oscillator circuits to generate phase shifts tunable with oscillator natural frequency. While these results are encouraging, optimizing the beam steering and ensuring phase relationships between neighboring elements compels the adaptation of phase-locking circuits to the practical implementation of coupled oscillator phased arrays.

A CPLL phased-array antenna can be constructed with oscillators phase locked through a feedback network. In the simplest case, each oscillator is locked to its nearest neighbors. While offering phase control without the use of phase shifters, the dynamics of this system are essentially nonlinear due to the synchronization process. To this end, we reduce the scenario to two CPLLs and develop the relationship between the circuit parameters and synchronization. While the injection-locking featured in [1] and [9] is possible, the direct feedback path dominates the synchronization behavior.

The pertinent design goal of a CPLL circuit is reaching and maintaining stable locked operation. As is generally discussed with conventional phase-locked loops (PLLs), the synchronization of the oscillator depends on the pull-in range. This range is considered as the set of frequency detuning that eventually lead to lock. The hold-in range reflects the robustness of the locked state. This range is the set of frequency detuning for which the circuit remains in lock [3]. From this description, it is clear that the hold-in range is an upper bound on the pull-in range. In general, the pull-in characteristics are a feature of the global stability of the system, while the hold-in characteristics are a feature of its local stability.

While understanding the effect of circuit parameters (such as gain) on the hold and pull-in ranges is crucial to CPLL design, demonstrating the influence of propagation delay on bidirectional coupled oscillators is also of interest. This paper demonstrates the limitation of time delay on the open loop gain of the CPLL. As a result, the propagation delay is an important design constraint in a practical CPLL phased-array implementation. Research on optical PLLs has demonstrated the tradeoff between delay, bandwidth, and gain [10], [11] in the presence of noise. This paper studies the stability tradeoffs of these parameters in the context of coupled oscillators.

II. CPLL Model

A simple physical description of a CPLL is adequate for explaining much of the observed behavior. Fig. 1 suggests the follow system of equations for each PLL:

$$\begin{aligned} \tau_p \dot{y}_i + y_i &= \alpha_i\left(\tau_{zi}\left(\dot{x}_{i-1} - \dot{x}_i\right) + \left(x_{i-1} - x_i\right)\right) \\ x_1 &= K_p \sin(\phi_2)\sin(\phi_1) \approx \frac{1}{2} K_p \cos\Delta\phi \\ \dot{\phi}_i &= \omega_i + K_v y_i. \end{aligned} \tag{1}$$

The first equation describes a passive first-order low-pass filter with pole and zero time constants τp and τz, respectively, and amplification α. The second equation describes the mixer, which multiplies two periodic signals with a gain of K_p, and produces an error signal. Other phase detectors can be considered, but our intent is to understand a simple loop model in the presence of a propagation delay and understand the impact on the synchronization behavior. The additional sum term is neglected because the low-pass filter suppresses its effect on the CPLL dynamics. Finally, the third equation is a linear model of the voltage-controlled oscillator (VCO), characterized with natural frequency ωi and a tuning sensitivity K_v. The tuning sensitivity for each oscillator is assumed to be identical, but the natural frequencies are allowed to differ. The phase output ϕ represents the argument of the locked signal. Note that the CPLL in Fig. 1 reduces to a PLL if the amplification of either loop filter is set to zero.

Manuscript received February 20, 2002. This work was supported by the Office of Naval Research under Grant N0014-00-1-0015.

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Digital Object Identifier 10.1109/TMTT.2003.808701

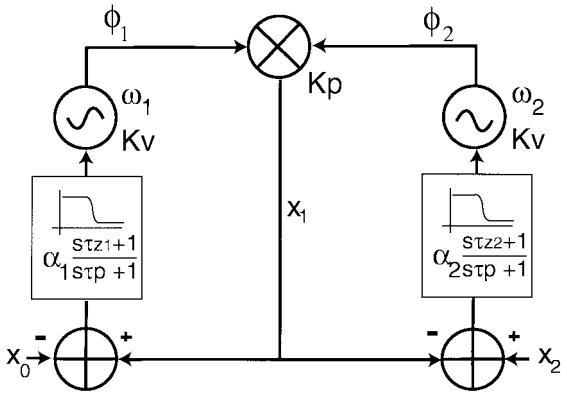

Fig. 1. CPLL topology.

From the set of equations in (1), the evolution of the phase difference $\Delta\phi = \phi_2 - \phi_1$ between the PLLs may be derived as follows:

$$\tau_p \Delta\ddot{\phi} + (1 + (\tau_{z1} G_1 + \tau_{z2} G_2) \sin\Delta\phi)\, \Delta\dot{\phi} - (G_1 + G_2) \cos\Delta\phi = \Delta\omega - f(x_0, x_2, \dot{x}_0, \dot{x}_2) \quad (2)$$

where $G_i = 1/2\alpha_i K_v K_p$ and $\Delta\omega = \omega_2 - \omega_1$.

G_i is referred to as the dc open loop gain with units of radians per second, and $\Delta\omega$ as the frequency detuning between the two PLLs. At this point, let us ignore the impact of external modulation, i.e., $f(x_0, x_2, \dot{x}_0, \dot{x}_2) = 0$. Defining $\xi_1 = \Delta\phi$ and $\xi_2 = \Delta\dot{\phi}$, (2) is cast as the following system of first-order ordinary differential equations (ODEs):

$$\begin{aligned} \dot{\xi}_1 &= \xi_2 \\ \tau_p \dot{\xi}_2 &= -(1 + \mu \sin\xi_1)\, \xi_2 + G\cos\xi_1 + \Delta\omega \end{aligned} \quad (3)$$

where $\mu = (\tau_{z1} G_1 + \tau_{z2} G_2)$ and $G = G_1 + G_2$.

The desired behavior of the CPLL is phase locking of the constituent PLLs. Mathematically, this behavior corresponds to solutions such that $\dot{\xi}_1, \dot{\xi}_2 = 0$. Solving (3), equilibrium points exist at

$$\bar{\xi}_{\text{eq}} = \begin{cases} \begin{bmatrix} \cos^{-1}\left(\dfrac{-\Delta\omega}{G}\right) \\ 0 \end{bmatrix}, & \xi_{\text{eq1}} \in (0, \pi) \\ \begin{bmatrix} \sin^{-1}\left(\sqrt{1 - \left(\dfrac{\Delta\omega}{G}\right)^2}\right) \\ 0 \end{bmatrix}, & \xi_{\text{eq1}} \in (\pi, 2\pi). \end{cases} \quad (4)$$

This implies that, at a given gain and frequency detuning, two equilibrium points exist. For instance, zero frequency detuning results in equilibrium points for $+/-90^\circ$. However, existence does not guarantee stability; the observed behavior of the CPLL will depend on the stability of the equilibrium points.

The eigenvalues of the Jacobian matrix $J(x)$ determine the local stability of the equilibrium and effectively define the hold-in range. The Jacobian matrix associated with the equilibrium points of the CPLL is determined to be

$$J(\xi_{\text{eq}}) = \begin{bmatrix} 0 & 1 \\ -\dfrac{1}{\tau_p} G \sin\xi_{\text{eq1}} & -\dfrac{1}{\tau_p}(1 + \mu\sin\xi_{\text{eq1}}) \end{bmatrix} \quad (5)$$

with eigenvalues satisfying the following quadratic equation:

$$\lambda^2 + \frac{1}{\tau_p}(1 + \mu\sin\xi_{\text{eq1}})\,\lambda + \frac{G}{\tau_p}\sin\xi_{\text{eq1}} = 0. \quad (6)$$

The solutions to (6) provide the following conclusions about the equilibrium points of the CPLL.

- The fixed point $\xi_{\text{eq1}} \in (0, \pi)$ will always be linearly stable.
- The fixed point $\xi_{\text{eq1}} \in (\pi, 2\pi)$ will always be unstable.

Behavior at 0 and π is more complicated, but, from a practical standpoint, can be ignored since, in the presence of noise, the observed stability boundaries of the CPLL are reduced from those predicted by (4).

The range of frequency detuning satisfying the stable equilibrium point characterizes the hold-in range. The hold-in range can be quantified from the argument in (4) as follows:

$$\Omega_h = 2G. \quad (7)$$

Comparing this result to a conventional PLL demonstrates that the CPLL has a hold-in range that is simply the summation of hold-in ranges of the constituent PLLs.

A measurement of hold-in range is useful for calculating the open loop gain and does not require breaking the feedback loop. To validate this measurement, the circuit must synchronize over the entire range of phase.

Estimating the pull-in range for a CPLL is critical to ensure phase locking. An estimate of the pull-in range for a PLL is [4]

$$\Omega_p \approx 2\sqrt{\frac{G^2\tau_z + G}{\tau_p}}. \quad (8)$$

Unfortunately, the pull-in process for a PLL or CPLL is difficult to solve for exactly since it involves a global estimation of the circuit behavior. Since trajectories of (3) are periodic, we assume a first-order relationship between the state variables

$$\xi_2 = a + b\cos\xi_1 + c\sin\xi_1. \quad (9)$$

Dividing the two state equations in (3) gives an expression for the trajectories in the phase plane as follows:

$$\tau_p \frac{d\xi_2}{d\xi_1} = -(1 + \mu\sin\xi_1) + \frac{1}{\xi_2}(G\cos\xi_1 + \Delta\omega). \quad (10)$$

For ease of estimation, we assume the loop filter has no zero. In that case

$$\begin{aligned} d.c. : a &= \Delta\omega \\ \sin\xi_1 : \tau_p ab &= c \\ \cos\xi_1 : \tau_p ac &= -b + G \\ \rightarrow a &= \Delta\omega \\ b &= \frac{G}{1 + (\tau_p\Delta\omega)^2} \\ c &= \frac{\tau_p\Delta\omega G}{1 + (\tau_p\Delta\omega)^2}. \end{aligned} \quad (11)$$

The maximum $\Delta\omega$ that results in (9) intersecting the ξ_1-axis is an approximation for the boundary of the pull-in range. Graphically, this is demonstrated in Fig. 2. Trajectories that cross the axis generally result in lock. In Fig. 2, the maximum

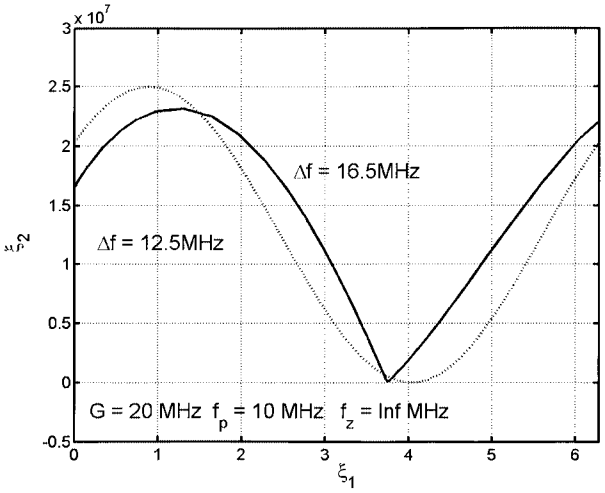

Fig. 2. Comparison of simulated capture trajectory (black trace) of system described in (3) and first-order trajectory (gray trace) described in (9). The frequency detunings that mark the boundary of these trajectories are noted in the graph.

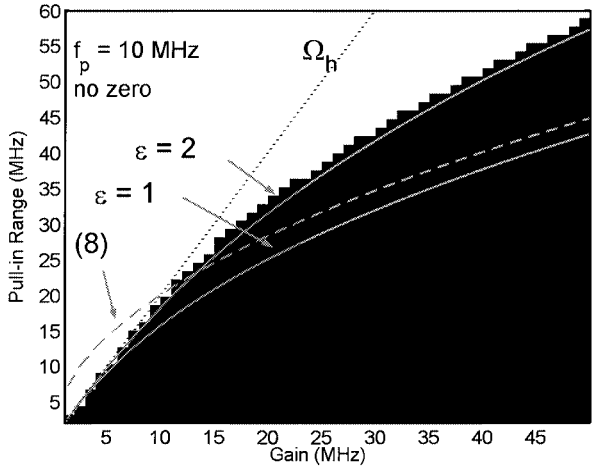

Fig. 3. Pull-in range versus gain. The dark region represents the locked state calculated from a numerical simulation of (3). The gray lines are the analytic expressions derived in (13) and (15) compared with the expression given in (8). The hold-in range is also provided for reference.

capture trajectory sharply turns away from the axis. It follows for (9) that ξ_2 must, for some a, b, and c, be nonnegative for all ξ_1. At the point of contact with the axis, the first-order relationship has a minimum. Hence, the conditions on (9) are

$$\xi_2 \geq 0 \text{ and } \frac{d\xi_2}{d\xi_1} = 0. \tag{12}$$

Reducing the expressions in (12) and substituting our values of a, b, and c from (11) into this expression, the maximum $\Delta\omega$ can be calculated; the pull-in range is approximated as twice this frequency detuning as follows:

$$\Omega_p \simeq 2\sqrt{\frac{\sqrt{1+4\tau_p^2G^2}-1}{2\tau_p^2}}. \tag{13}$$

The limit of this expression for a large pole time constant or gain is identical to (8) when the zero is removed. Additionally, the limit of this expression as the pole time constant goes to zero is equivalent to a PLL with no loop filter. In this case, the pull-in range should be identical to the hold-in range [3]. In the framework of (1), we are setting the zero and pole time constants equal. This limit can be calculated with an expansion for the square root as follows:

$$\Omega_p \simeq \lim_{\tau_p \to 0} \frac{2}{\tau_p}\sqrt{\frac{1+\frac{1}{2}4\left(\tau_pG\right)^2-1}{2}} = 2G. \tag{14}$$

As expected, the pull-in range converges to the hold-in range for small pole time constants, which is the advantage of this expression over (8).

Since the approximation used to find this relationship involved a first-order harmonic balance, agreement with numerical results is limited. The conditions imposed in (12) are a rough approximation to the actual pull-in range boundary, and this is readily apparent from Fig. 2. Comparing Figs. 2 and 3 for the gain of 20 MHz, the actual pull-in range is 8 MHz greater than found with (13).

A better approximation can be reached by scaling the pole time constant according to (15). In Fig. 3, (3) is numerically integrated over a range of frequency detuning and gain and the resulting lock (unlock) is depicted with a black (white) region. We find the agreement between the simulated mesh and the analytic expression to be close over the entire range for epsilon equal to two. This corresponds with one-half the original pole value as follows:

$$\tau_p \to \frac{\tau_p}{\varepsilon} \quad \Omega_p = 2\sqrt{\frac{\sqrt{1+\frac{4\tau_p^2G^2}{\varepsilon^2}}-1}{\frac{2\tau_p^2}{\varepsilon^2}}}. \tag{15}$$

Justifying this factor in the analytic result is not apparent at this time. One possibility is the exact boundary trajectory of the pull-in range in Fig. 2 contains a derivative discontinuity. As a result, estimating the effect of the higher order terms with an effective pole time constant may be a reasonable approximation.

The equations suggested in (13) and (15) are intended to provide some intuition about the effect of the circuit parameters on the pull-in range. In a phased-array implementation, ensuring lock with the appropriate circuit parameters may be a useful operating technique.

III. Time-Delay CPLL Model

Time delay is an unavoidable consequence of the physical layout of the PLL. Designing a PLL and observing oscillator spectra similar to spurious oscillator spectra motivates considering additional nonlinearities in the model. As demonstrated in [5] and [6], time delay can generate instabilities in a PLL under certain gain and frequency detuning conditions. Consequently, the effect of time-delay on pull-in and hold-in range is a design constraint. The results of (7) and (15) indicate that increasing the loop gain improves both the pull-in and hold-in ranges. However, the following analysis demonstrates that gain cannot be arbitrarily large.

A PLL model can be modified to incorporate a lump sum time delay. If the time delays are asymmetric in the two loops,

then separate time-delay variables must be considered. In what follows, the delay is assumed identical in both loops and can be transformed as a single time delay in the shared feedback path. Under this assumption, the CPLL dynamical equation with time delay is given by

$$\tau_p \Delta\ddot{\phi}(t) + \Delta\dot{\phi}(t) + \mu\Delta\dot{\phi}(t-T)\sin\Delta\phi(t-T) - G\cos\Delta\phi(t-T) = \Delta\omega. \quad (16)$$

From this second-order ODE, we want to obtain a system of first-order ODEs similar to (3). Small time delays can be handled with a Padé approximation [7]

$$e^{-sT} \approx \frac{1-\frac{sT}{2}}{1+\frac{sT}{2}}. \quad (17)$$

Introducing time-delayed state variables and relating them to the variables used in (3) allows us to express the time-delay CPLL model as a four-dimensional system of equations [6] as follows:

$$\begin{aligned}
\dot{\xi}_1 &= \xi_2 \\
\tau_p\dot{\xi}_2 &= -\xi_2 - \mu\xi_4\sin\xi_3 + G\cos\xi_3 + \Delta\omega \\
\dot{\xi}_3 &= \frac{2}{T}(\xi_1 - \xi_3) - \xi_2 = \xi_4 \\
\tau_p\dot{\xi}_4 &= \frac{2\tau_p}{T}(\xi_2 - \xi_4) + \xi_2 + \mu\xi_4\sin\xi_3 - G\cos\xi_3 - \Delta\omega.
\end{aligned} \quad (18)$$

As demonstrated in Section II, stable equilibrium points exist at

$$\bar{\xi}_{\text{eq}} = \begin{bmatrix} \cos^{-1}\left(\frac{-\Delta\omega}{G}\right) \\ 0 \\ \cos^{-1}\left(\frac{-\Delta\omega}{G}\right) \\ 0 \end{bmatrix}. \quad (19)$$

The unstable equilibrium points are ignored since they do not contribute to the hold-in range. It is immediately evident from (19) that we should expect the same hold-in range as given in the original model without time delay. A caveat to this result is that the sum frequency mixer product is ignored in (1). When this term is included the effect of time delay on the hold-in range depends on the order of the PLL. For the assumed second-order loop, there is practically little effect on the hold-in range [8].

Stability of the phase-locked solutions can be determined from the eigenvalues of the Jacobian of (18) evaluated at (19). Previously, we found the one equilibrium point was stable for all circuit parameter values; however, this is not the case for the time-delay model and linear instability limits the range of stable phase differences. The calculation of the eigenvalues is greatly simplified by first making the transformation

$$\xi_2' = \frac{1}{2}(\xi_2 + \xi_4) \quad \xi_4' = \frac{1}{2}(\xi_2 - \xi_4).$$

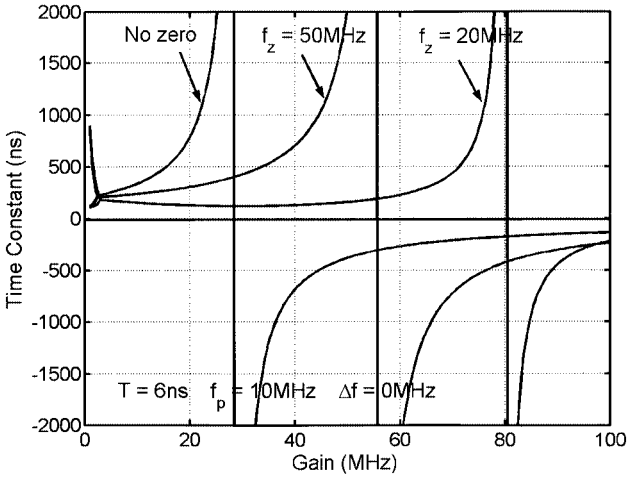

Fig. 4. Acquisition time constant versus gain for three different zero frequencies of the system described in (18). All three situations feature a singularity above which the CPLL no longer locks into a stable locked state.

The resulting Jacobian matrix evaluated at (19) is readily found to be

$$J(\xi_{\text{eq}}') = \begin{pmatrix} 0 & 1 & 0 & 1 \\ 0 & 0 & 0 & J_{2,4} \\ 0 & 1 & 0 & -1 \\ 0 & J_{4,2} & J_{4,3} & J_{4,4} \end{pmatrix} \quad (20)$$

where

$$\begin{aligned}
J_{2,4} &= \frac{2}{T} \\
J_{4,2} &= -\frac{(1+\mu)}{\tau_p} \\
J_{4,3} &= -\frac{G\sin\xi_{\text{eq3}}}{\tau_p} \\
J_{4,4} &= -\frac{2}{T} - \frac{(1+\mu\sin\xi_{\text{eq3}})}{\tau_p}
\end{aligned}$$

and

$$\sin\xi_{\text{eq3}} = \frac{\sqrt{G^2 - \Delta\omega^2}}{G^2}.$$

One eigenvalue is zero, while the remaining three eigenvalues are roots of the following cubic equation:

$$\lambda^3 + a\lambda^2 + b\lambda + c = 0 \quad (21)$$

where

$$a = -J_{4,4} \quad b = J_{4,3} - J_{2,4}J_{4,2} \quad c = -J_{2,4}J_{4,3}$$

and Cardano's method may be used to obtain these roots. Fig. 4 displays the eigenvalue behavior of (21) as a time constant for the decay of a trajectory to the equilibrium point. Notice time-constant behavior in Fig. 4 is qualitatively similar for any zero frequency. To simplify analysis, we assume there is no zero in the CPLL. One important feature of Fig. 4 is the singularity associated with a critical gain. Once the time constant becomes negative, the PLL will no longer lock at constant phase. The PLL locks instead in a limit cycle to the injected signal. The resulting frequency instability regions are described in [5]. The limit cycle is a periodic response with period related to circuit parameters.

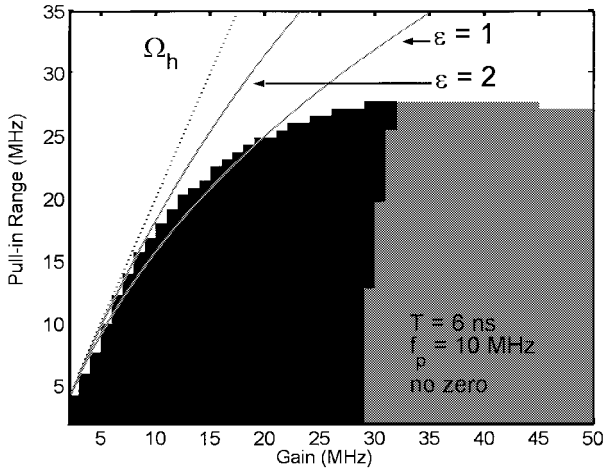

Fig. 5. Pull-in range versus gain for the time-delay CPLL model. The two regions correspond to a different locking behavior: the dark region represents a stable locked state and the gray region represents locking to a periodic phase. The values of epsilon are plotted from (15).

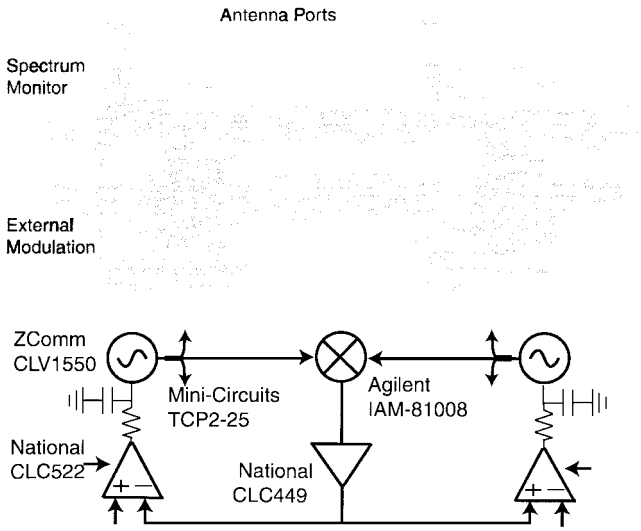

Fig. 6. Circuit implementation for CPLL. Each board in the top figure represents an individual PLL that is coupled to its neighbor via the RF path and the low-frequency feedback path.

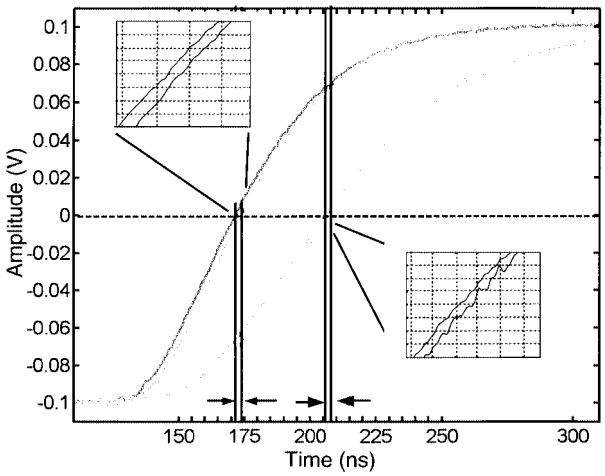

Fig. 7. Measured time delay in the open loop. Inset figures have a scale of 5 ns/div and 5 mV/div. The four traces correspond to the waveform at a different point in the loop. The largest delay results from the loop filter, while the insets demonstrate a 6-ns propagation delay through the amplifiers and mixer.

Finally, Fig. 4 also demonstrates that the critical gain occurs at the lowest gain when there is no zero in the loop. As the zero frequency approaches the pole frequency, the critical gain increases until it reaches a maximum for a zero of 20 MHz. The critical gain decreases from this value until it reaches 70 MHz when the pole and zero frequencies are equal.

Estimating the pull-in range of (18) is considerably more involved. A reasonable analytic solution is difficult to reach. Reference [4] offers an approach using a functional minimum. For qualitative understanding, consider numerically solving (18). Fig. 5 provides a direct comparison with Fig. 3 to understand the effect of time delay on pull-in range. For small gains, the graphs are similar. Around 15 MHz, the range in Fig. 5 rolls off and, for higher gains, the numerical simulation demonstrates that the pull-in range is not monotonic, but peaks at a gain of 30 MHz.

The two tones of Fig. 5 represent two different locking behaviors. The dark region represents locking to a steady-state phase. The gray region represents locking to a limit cycle resulting from the critical gain instability.

A few additional comments can be made about the instability comparing the matrix elements of (20) to Figs. 4 and 5. First, gain and frequency detuning are related. The instability occurs at the lowest gain for zero detuning. Larger detuning effectively decreases the gain. This is evident in Fig. 5. The gray (limit cycle) region extends to the lowest gain for small pull-in conditions (frequency detuning). The graph in Fig. 4 is the worst case for instability; larger frequency detuning would shift the singularities right. Second, the time constant can increase with gain implying that pull-in can actually take longer for higher gains.

Time delay changes the expected synchronization behavior of the CPLL and the analysis provides considerations for the pull-in and hold-in behavior. A frequency instability that must be avoided in a potential CPLL phased-array circuit has been described in terms of limits on the gain.

IV. Measurement and Verification of CPLL Behavior

The circuit consists of a mixer, buffer, variable gain amplifier (VGA), and VCO, as shown in Fig. 6. The parts are referenced by the manufacturer and number. The buffer prevents bias point changes on the Gilbert cell mixer circuit. The VGA provides gain and voltage offset control, allowing variation of gain and frequency detuning. The dominant pole of the loop is introduced by an *RC* filter at the tuning input of the VCO. The pole frequency is 10 MHz and the filter does not include a zero. No external modulation is introduced in the measurement of the hold-in and pull-in ranges ($x_0 = x_2 = 0$).

The time delay results from the intrinsic transit and charging times of the devices and layout topology. The delay is expected to be 7 ns, comprising the total step response delay from the specifications of the amplifiers and the delay introduced by the signal path in the loop.

The measured time delay is approximately 6.0 ns, as seen in Fig. 7, over the range of gain values. The time delay is measured by following a step response through the open loop system. The loop is broken at the input to the VGA and a step voltage is

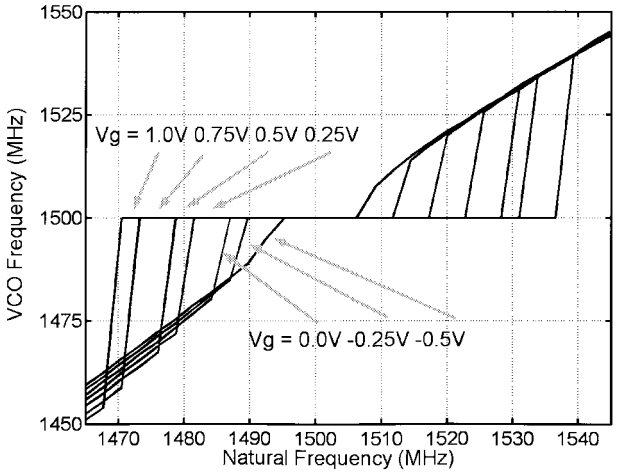

Fig. 8. Measured hold-in range for a single PLL at various loop gains referenced by the VGA control voltage.

applied to this input. The waveform at the VGA input is the darkest line. The increasingly lighter-colored waveforms are the output of the VGA, input to the VCO, and output of the buffer. The periodic signal apparent on the waveform at the output of the buffer is related to the sum frequency harmonic.

The nature of true time delay is, however, different than phase delay. The *RC* response is accounted for in the time constants of (3) and (18). Our approach has been to include another filter in the form of (17) to approximate the time delay. This approximate filter is quite different from the loop filter because it features a right half-plane (RHP) zero instead of a left half-plane zero. RHP zeros introduce instability in the feedback as illustrated in the eigenvalue behavior of Fig. 4. The RHP zero occurs because the Bode response of true time delay is essentially a flat magnitude response (all-pass) over all frequencies with a linear decrease in phase. As a result, the effect of true time delay is a shift of the waveform in time, as seen in the measured waveforms, while the *RC* time constant changes the slope of the waveforms.

A hold-in range measurement of the PLL cell determines the gains of the PLL and CPLL circuits. The PLL hold-in range can be measured from the CPLL with one amplifier set to zero gain. Fig. 8 illustrates the PLL hold-in range at several gain control voltages. The VGA offers gain control voltages corresponding to the dc loop gain in the following plots. These gain control voltages vary from -1 to 1 V. The loop gain can be calculated from the hold-in range with (7). Table I lists the corresponding dc loop gain for measured PLL hold-in ranges.

Assuming a CPLL consists of two identical PLLs, we expect that the dc loop gain of the CPLL is twice that of the PLL. Therefore, the hold-in range for the CPLL should be four times the loop gain of the PLL. For instance, $Vg = 0.0$ V has a PLL hold-in range of 30 MHz in Fig. 8. This indicates that the loop gain is 15 MHz. When two identical PLLs are coupled, the loop gain is 30 MHz and the hold-in range of the CPLL should be 60 MHz.

A. Hold-In Range

From the PLL measurements, the hold-in range is anticipated in Table I. Fig. 9 is a measurement of the hold-in range for the

TABLE I
GAIN AND HOLD-IN RANGES FOR VARIOUS GAIN CONTROL VOLTAGES IN THE PLL AND CPLL CIRCUITS

Vg (Volts)	Measured PLL Hold-in Range (MHz)	G1; G2=0 (MHz)	G; G1=G2 (MHz)	Expected CPLL Hold-in Range (MHz)
-0.5	12	6	12	24
-0.25	22	11	22	44
0.0	30	15	30	60
0.25	41	20.5	41	82
0.5	50	25	50	100
0.75	58	29	58	116
1.0	66	33	66	132

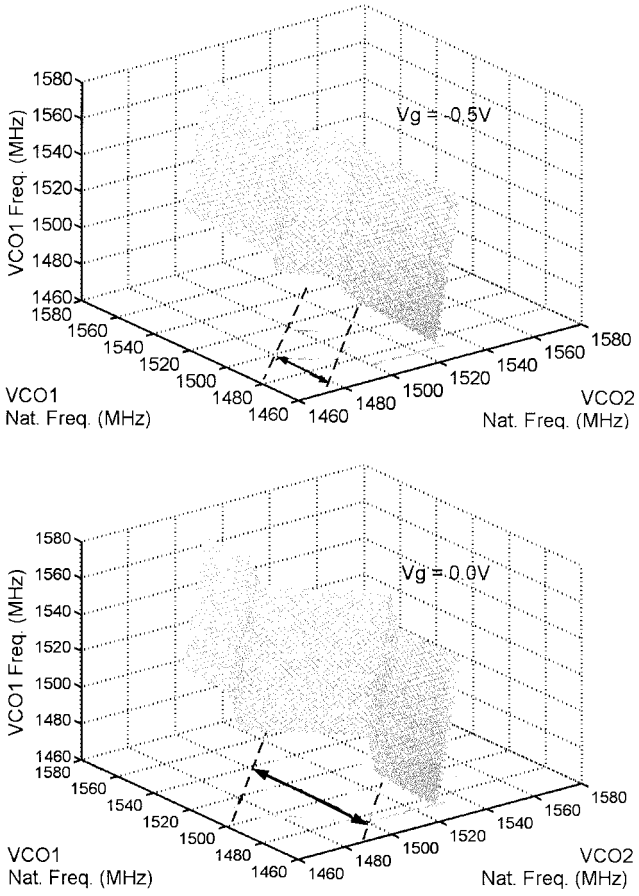

Fig. 9. Measured hold-in ranges of the CPLL at two different loop gains versus the natural frequencies of the oscillators. The level face of the graph demonstrates the locked state.

CPLL circuit. The natural frequencies are set equal (zero detuning) to ensure that the oscillators are initially locked. Subsequently, each natural frequency is stepped transversely away from the zero detuning condition. The steps are intended to approximate continuous movement from zero detuning and allow an accurate measurement of the local stability. The frequency of an oscillator is measured at each set of natural frequencies to generate a curve that is a three-dimensional extension to the hold-in range in Fig. 8.

Two values of gain are presented for comparison with Table I. The first measurement is made with $Vg = -0.5$ V. Each loop has a loop gain of 6 MHz and the hold-in range for the CPLL should be twice the combined gain or 24 MHz. From the upper

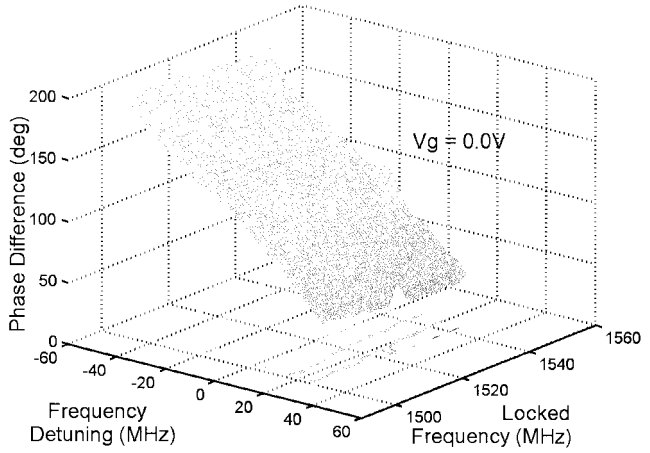

Fig. 10. Relative phase difference versus the frequency detuning and locked frequency of the CPLL oscillators at $Vg = 0.0$ V.

graph in Fig. 9, the double-headed arrow marks the distance between the dashed lines, which reference the contour boundary of the hold-in range. The arrow spacing is (1500–1467) or 33 MHz. The geometry of the graph, however, implies that this spacing is the hypotenuse of a right isosceles triangle and the actual hold-in range is one side of this triangle. Consequently, the measured hold-in range is 33 MHz divided by root 2 equaling 23.3 MHz, close to the expected value.

The second measurement is made with $Vg = 0.0$ V. Table I anticipates a hold-in range of 60 MHz. The arrow spacing in the lower graph is approximately 72 MHz. By the same method, this value is divided by root 2 and the measured hold-in range is 52 MHz. This measurement illustrates greater discrepancy between the theory and measurement.

To address the difference, consider that the correspondence between the hold-in range and the loop gain is contingent on the full phase range. Fig. 10 is an example of the phase plane curve corresponding to the high gain case in Fig. 9. The time delay between the VCO signals is sampled with an 8-GS/s oscilloscope to give the phase difference. The region illustrated is limited to the actual hold-in range.

The primary feature of the phase curve is the small range of phase differences that are not present. The phase curve reaches within $+/-10$ degrees of the boundary of the hold-in range, producing a hold-in loss of 4 MHz. This results, in part, from the nature of the measurement. Circuit noise prevents reaching the boundary of the hold-in range without losing lock. The hold-in measurement requires stepping the tuning voltage of two oscillators. In particular, the natural frequency is stepped by approximately 1 MHz. This step can break the lock before the boundary is reached. The PLL measurement of Fig. 8 was less sensitive to this effect because only one oscillator is swept.

B. Pull-In Range

The analysis for pull-in range of the time-delay CPLL model is limited to simulation. Agreement between Fig. 5 and the measurement of the pull-in range justifies the time-delay model. The measurement begins by setting a large frequency detuning to ensure the oscillators are not initially locked. The natural

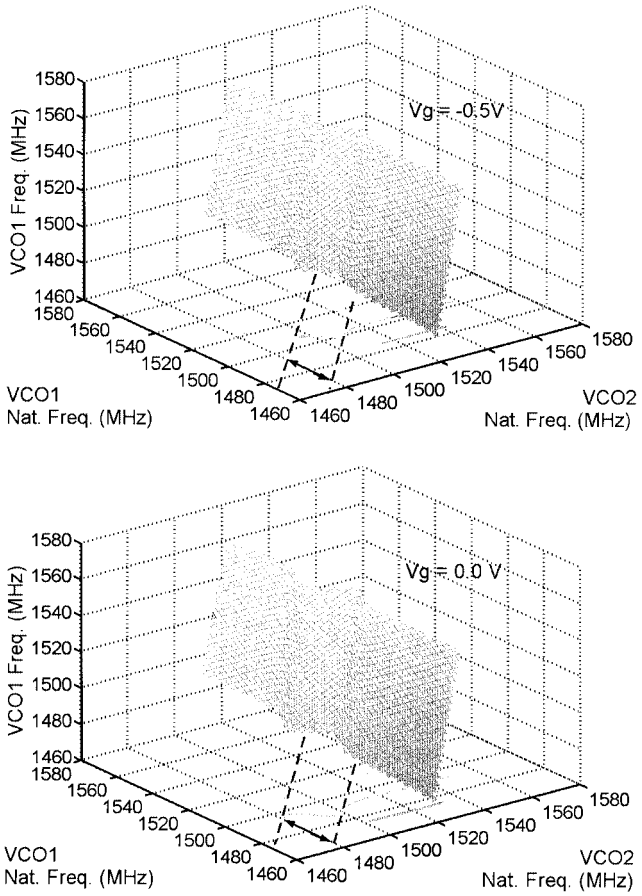

Fig. 11. Measured pull-in ranges of the CPLL at two different loop gains versus the natural frequencies of the oscillators.

frequencies are swept transversely toward zero detuning. The resulting curve is qualitatively similar to the hold-in range curve, but reduced, as is expected, since the pull-in range is smaller than the hold-in range.

The same values of gain are presented for comparison with Figs. 9 and 11. As before, the loop gain of the CPLL is 12 MHz for $Vg = -0.5$ V. The expected pull-in range for the CPLL is approximately 18 MHz from Fig. 5. From the upper graph in Fig. 10, the double-headed arrow marks the distance between the dashed lines provided to illustrate the boundary of the pull-in range. The arrow spacing is (1493–1467) or 26 MHz. As before, the actual pull-in range is scaled and this gives 26 MHz divided by root 2 equaling 18.4 MHz, close to the value found in the numerical simulation on the time-delay CPLL model. Comparing this result with Fig. 9, the pull-in range is about 3/4 of the hold-in range for this gain and pole frequency.

The second measurement is made at $Vg = 0.0$ V or a gain of approximately 30 MHz. Fig. 5 anticipates a pull-in range of 27 MHz. The spacing of Fig. 11 is approximately 34 MHz. By the same method, this gives a pull-in range of 24 MHz. This is reasonably close to the expected value. The resulting ratio of pull-in to hold-in range is 0.4. This measurement justifies considering the effect of time delay on the pull-in range. Fig. 5 is a more accurate picture of the pull-in behavior than Fig. 3.

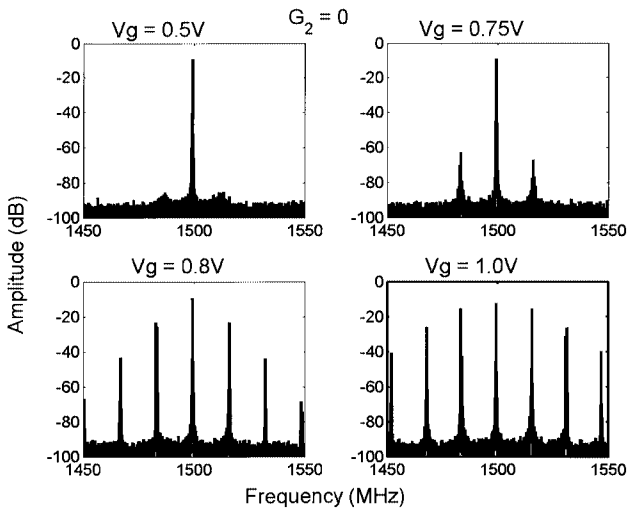

Fig. 12. PLL frequency spectra for increasing loop-gain values. The harmonic lobes increase in power drastically between the 0.75–0.8-V measurements.

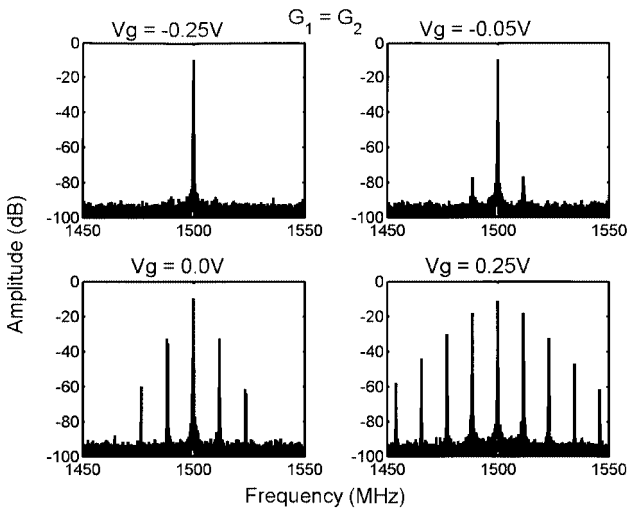

Fig. 13. CPLL frequency spectra at increasing loop-gain values. The behavior is similar to the PLL case, however, the loop-gain values are different reflecting the influence of the coupled dynamics.

C. Time-Delay Instability

From the discussion in Section III, the critical gain is the gain at which a stable equilibrium point becomes unstable. For higher gain, the loop locks to a limit cycle, i.e., the phase difference between the PLLs oscillates rather than settling to a constant value. The manifestation of this behavior in the circuit is the spurious harmonic content in the VCO carrier frequency.

Fig. 12 is a spectrum measurement of the PLL at several different gains. The CPLL is uncoupled, as done to measure the PLL locking range, and the gain is increased to display the bifurcating response. For low gain, the carrier signal features the suppressed noise floor characteristic of the PLL. Near the critical gain, two spurious harmonics appear. These harmonics are related to the limit cycle described in Section III. While they are still 70 dB below the carrier, a small increase in gain brings these harmonics within 20 dB of the carrier. At still higher gains, the harmonic content is considerable and the power in the harmonics is on the order of the carrier.

Weak sidelobes in the spectra in Figs. 11 and 12 may appear below the critical gain because noise sources in the loop excite this harmonic response. Therefore, the critical gain is referenced to a point when the harmonic power increases drastically rather than the initial appearance of lobes.

Fig. 12 illustrates that the critical gain occurs near $Vg = 0.75$ V. From Table I, the loop gain of the PLL is 29 MHz. Referring to Fig. 4, the critical gain for a PLL without a zero is anticipated at 28 MHz. This demonstrates good agreement for the first-order approximation of the time delay. The discussion of time-delay instability determined that given the critical gain for the PLL remains the same for the CPLL. This implies that each loop contributes half as much gain so the total contribution conserves the critical gain.

Fig. 13 is a measurement of critical gain for the CPLL circuit. The critical gain occurs slightly below the $Vg = 0.0$ V. From Table I, this voltage corresponds with loop gain of 30 MHz. As expected, the critical gain remained unchanged between the PLL and CPLL.

V. Conclusion

A phased-array design based on CPLL circuits motivates understanding the relationship between circuit parameters and the synchronization process. Practical experience compels the inclusion of loop time delay and its effect on the hold-in and pull-in ranges has been studied. Time delay introduces circuit instability associated with a critical gain. While higher gain can improve the hold-in and pull-in range, neighboring oscillators will not maintain a stable phase relationship. A 1.5-GHz CPLL demonstrated agreement with the hold-in and pull-in range analysis and displayed the predicted critical gain behavior.

While the analysis and experimental circuits have been reduced to a two CPLL case, the approach can be extended to larger arrays to demonstrate a phased-array antenna system. Additionally, locking to an external reference source could compensate for temperature and time drifts across an implemented array, as demonstrated in [9].

Acknowledgment

The authors appreciate the support and encouragement of B. Meadows, Space and Naval Warfare Systems Command Center (SPAWAR), San Diego, CA, and P. Maccarini, University of California at Santa Barbara, for his helpful discussions.

References

[1] R. A. York and T. Itoh, "Injection and phase-locking techniques for beam control," *IEEE Trans. Microwave Theory Tech.*, vol. 46, pp. 1920–1929, Nov. 1998.

[2] R. Pogorzelski, P. F. Maccarini, and R. A. York, "Continuum modeling of the dynamics of externally-locked coupled oscillator arrays," *IEEE Trans. Microwave Theory Tech.*, vol. 47, pp. 471–478, Apr. 1999.

[3] H. Meyr and G. Ascheid, *Synchronization in Digital Communications*. New York: Wiley, 1990.

[4] S. Moridi and H. Sari, "Effect of loop delay on the pull-in range of generalized second order phase locked loops," in *Proc. IEEE Int. Communications Conf.*, vol. 2, June 1987, pp. 1041–5.

[5] W. Wischert, M. Olivier, and J. Groslambert, "Frequency instabilities in phase-locked synthesizers induced by time delay," in *Proc. IEEE Frequency Control Symp.*, May 1992, pp. 201–6.

[6] J. Buckwalter and R. A. York, "Time delay considerations in high-frequency phase-locked loop," in *IEEE RFIC Conf.*, June 2000, pp. 181–184.
[7] G. F. Franklin, J. D. Powell, and A. Emami-Naeini, *Feedback Control of Dynamic Systems*, 3 ed. Reading, MA: Addison-Wesley, 1994.
[8] N. Margaris and P. Mastorocostas, "On the nonlinear behavior of the analog phase-locked loop: Synchronization," *IEEE Trans. Ind. Electron.*, vol. 43, pp. 621–629, Dec. 1996.
[9] H.-C. Chang, X. Cao, U. K. Mishra, and R. A. York, "Phase noise in coupled oscillators: Theory and experiment," *IEEE Trans. Microwave Theory Tech.*, vol. 45, pp. 604–615, May 1997.
[10] R. T. Ramos and A. J. Seeds, "Delay, linewidth, and bandwidth limitations in optical phase-locked loop design," *Electron. Lett.*, vol. 26, no. 6, pp. 389–391, Mar. 1990.
[11] M. A. Grant, W. C. Michie, and M. J. Fletcher, "The performance of optical phase-locked loops in the presence of nonnegligible loop propagation delay," *J. Lightwave Technol.*, vol. 5, pp. 592–597, Apr. 1987.

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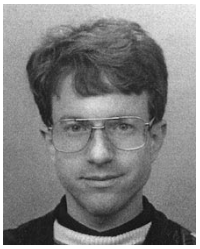

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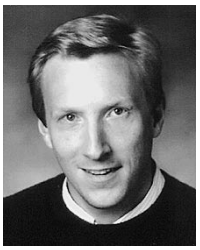

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